# Front end electronics for ATLAS pixel detector

L. Blanquart

# Front End electronics for ATLAS pixel detector

*L. Blanquart, CPPM*
*on behalf of the ATLAS pixel collaboration*

Overview of the ATLAS pixel detector

The demonstrator programme

The radiation-hard full arrays: FE-D & FE-H

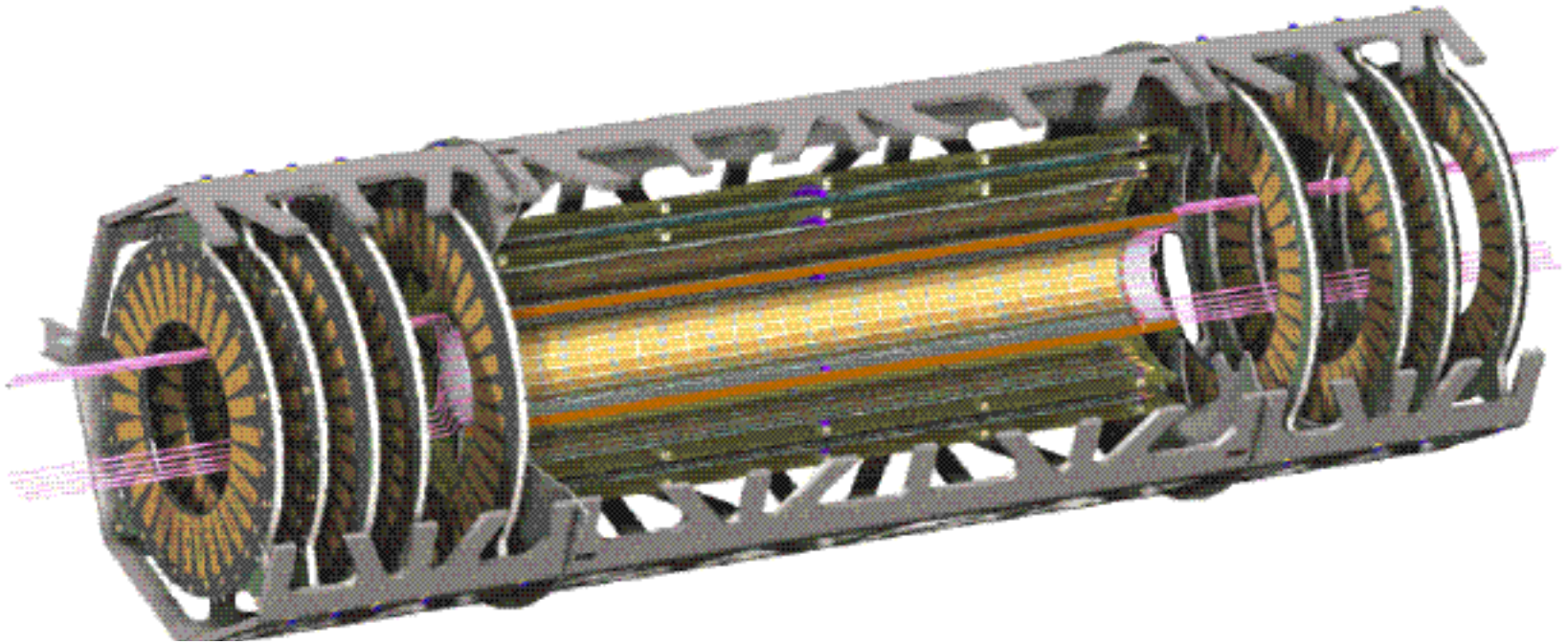
Concluding

# The ATLAS pixel tracker

The layout consists of 2 barrels at R=9.7 cm and 12.7 cm along with 5 discs in each of the forward regions plus a small radius replacable barrel at R=4.15 cm (B-layer).

This leads to a total active area of 2.3m$^2$ with 140 million pixels arranged into 2228 16-chip modules.

One FE chip contains 2880 channels with pitches of 50μm in rΦ and 400μm in the *z* direction. The B-layer differs from the rest of the system in that the *z* pitch is 300μm.



# Module integration

## Flex-Kapton Hybridization (”chip-down” approach)

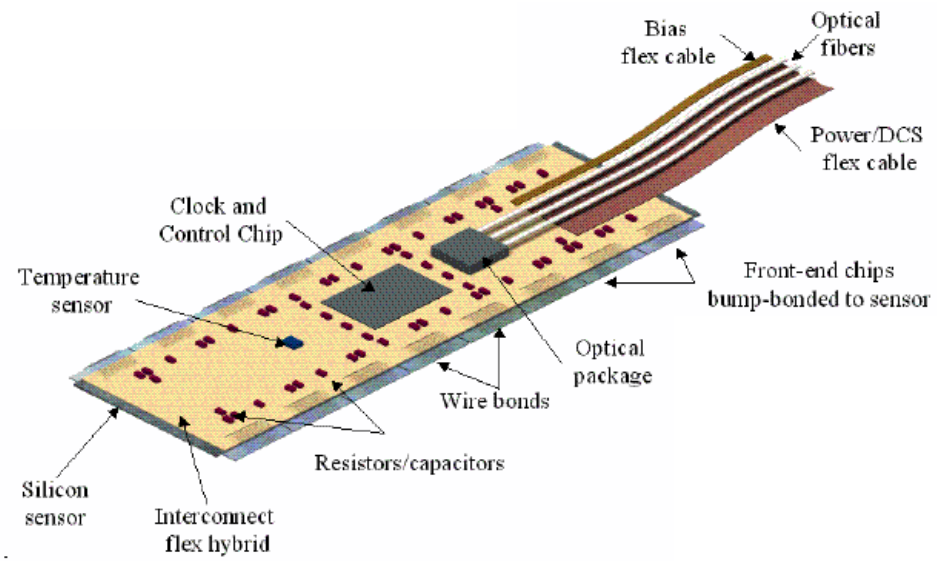
This is the baseline choise for the inner & outer layers + forward disks

FE chip backplanes are in direct thermal contact with the support structure.

The sensor (which is bump-bonded to the FE-chips) has the Kapton bussing piece glued to its backplane.

The FE chips protrude along the long edges of the sensor thus faciliting wire-bond connections up to the kapton hybrid

The Kapton layer has the role of supporting the Module Controller Chip (MCC) , optical transmission, reception devices, local decoupling..... along with distributing clocks/data between the MCC/FE.



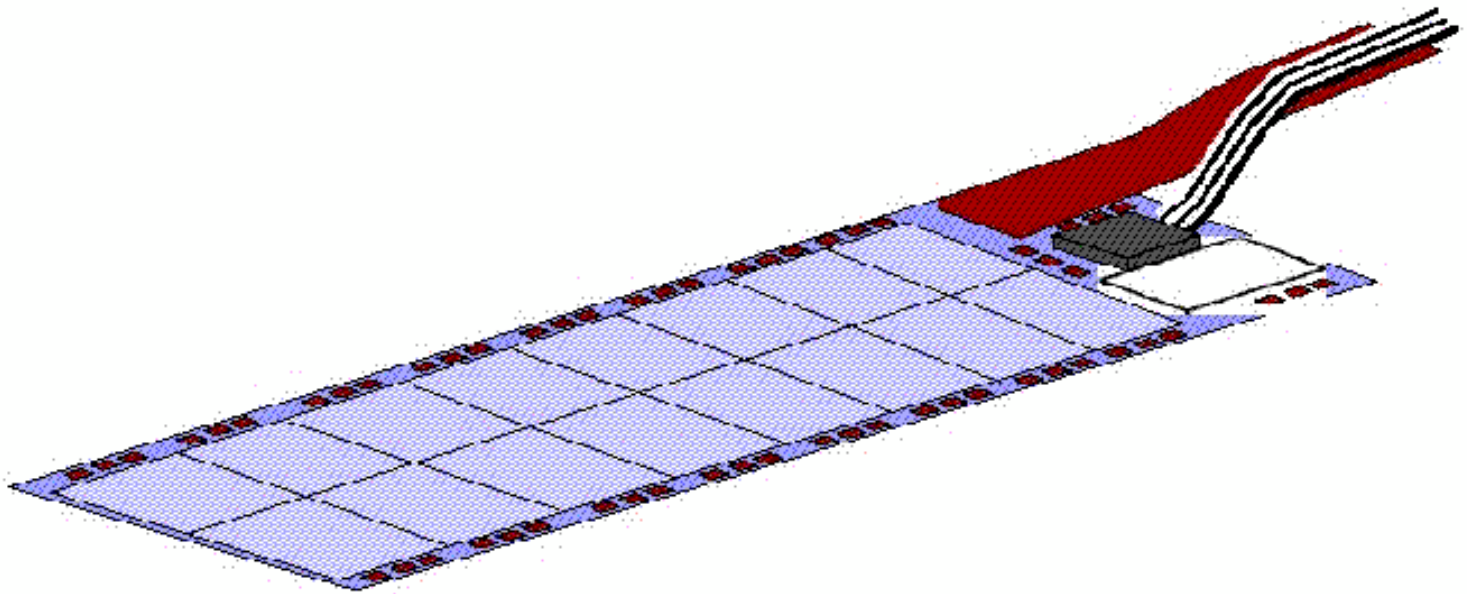
# Multi-Chip-Module-Direct (MCMD) Hybridization (”chip-up” approach)

This is the baseline choise for the B-layers.

Bussing structures and individual pixel via are actually fabricated on the surface of the sensor itself in up to 5-layers of Cu/BCB (post-production lithographic process)

MCC and other surface-mount components would be bump-bonded to the detector surface along with the FE chips thus eliminating wire-bonds

This strategy allows the sensor design for the B-layer to comprise unique pixel size, i.e. there is no need to gang or strech pixels at the chip boundaries hence hit ambiguities and degraded resolution are avoided for these regions.



# Module Controller Chip (MCC)

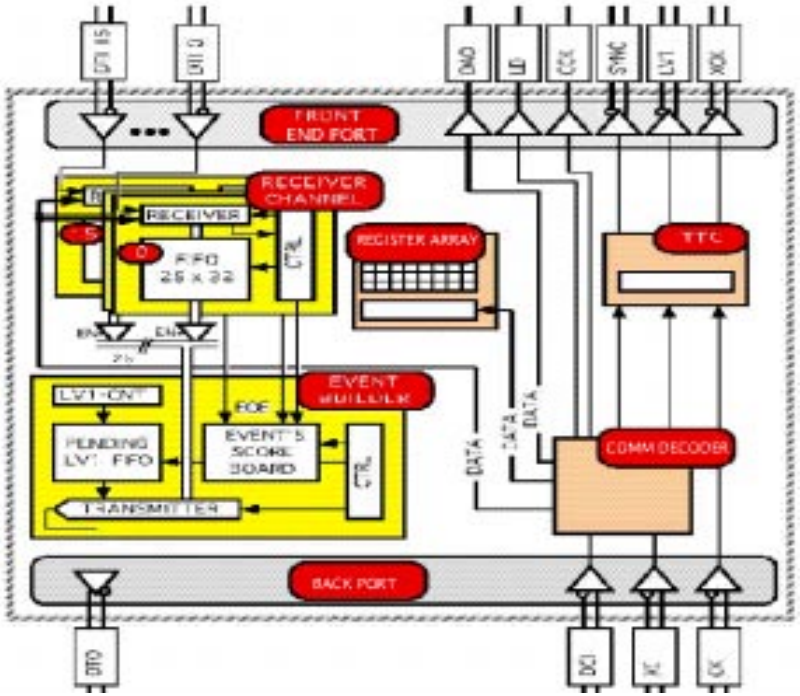
The Module Controller Chip (MCC) has the job of managing the data flow for one module (i.e. 16 FE chip system)

Responsibilities are summarised as:

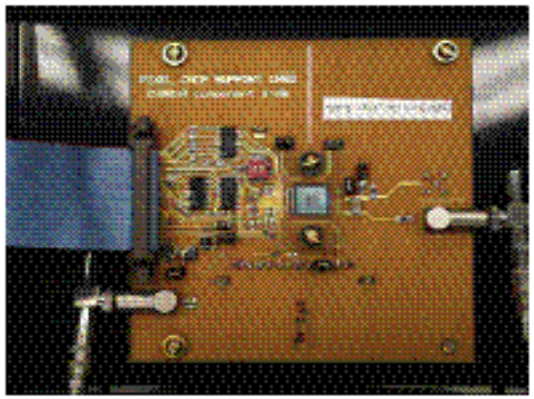
1. providing configuration information to the FE chips
2. serial data capture from the 16 FE, local 'event building' and serial transmission
3. fast signal (trigger) handling and FE timing management
4. error-condition recognition and reporting

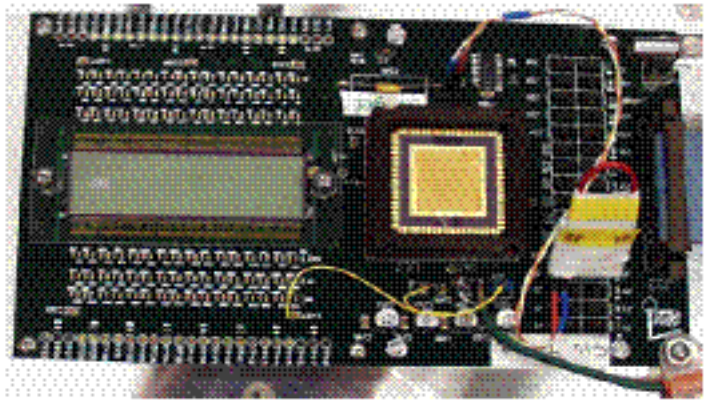
- AMS (rad-soft) prototypes have been tested on full-size modules in testbeams and in the laboratory using dedicated system; most features have been proven

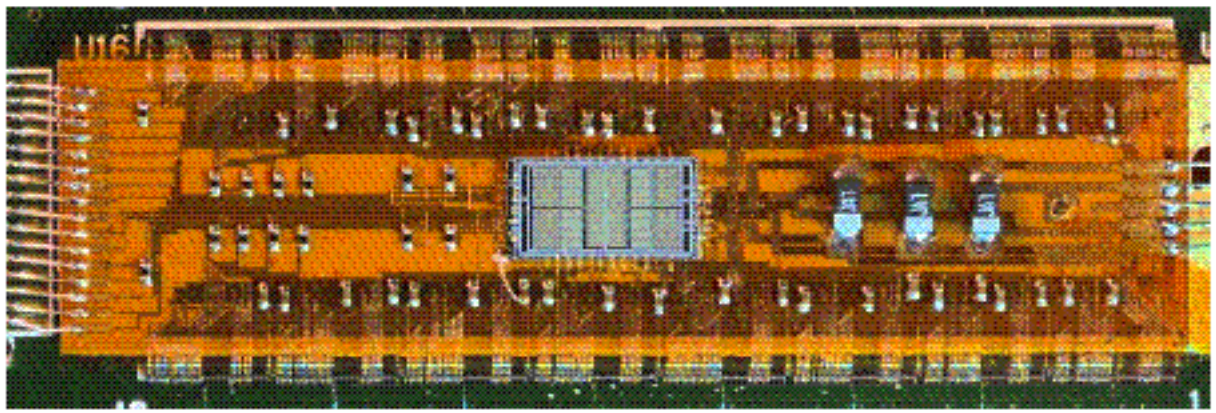
- reduced-functionality MCC has been implemented in radhard technology (DMILL) and successfully tested.

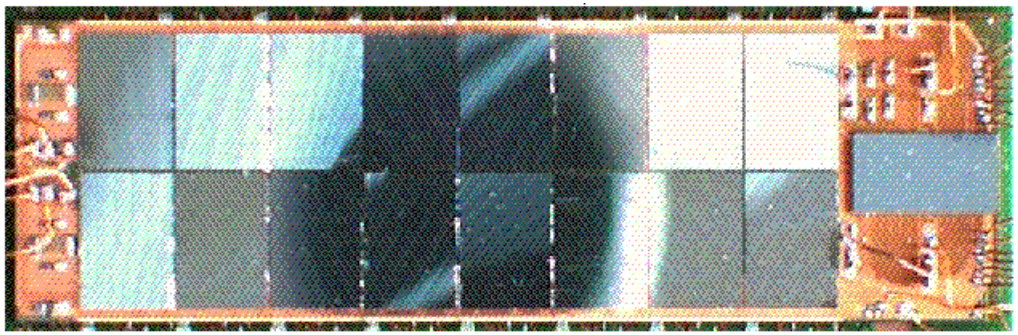


# Existing assemblies: photographs









# The Demonstrator Programme

## Introduction

- First 'proof of principle' chips were built in 96 and complete successfully by end of 97.

- The initial phase of this programme was aimed at realizing ATLAS specification FE-chips using radiation-soft technologies, the designs of which could then easily be adapted for fabrication at rad-hard foundries. First realistic prototypes were designed in 2 parallel efforts (Europe and US) in 97/98, producing a rad-soft AMS prototype (FE-A/FE-C) and a rad-soft HP prototype (FE-B).

- Throughout 98 & 99, >60 single chip assemblies and 10 electrically functional modules were produced and these have been studied extensively in the laboratory and during 7 testbeam periods at SPS.

- All of the ATLAS-requirement issues were addressed in detail such as noise, threshold dispersion, timing dispersion, timewalk, digital/analogue crosstalk, power supply rejection etc... with very encouraging results (see later)

- In parallel, reduced fonctionality prototypes have been implemented in radhard processes (DMILL & Honeywell SOI) to study performance and radiation hardness.

# Ultimate requirements

- Hit efficiency of >97% accounting for single channel failures, bump defects, timewalk, deadtime, charge division, radiation damage...

- Cope with $\cong$ 25 interactions/crossing at design luminosity, i.e. a pixel occupancy of $\cong 10^{-4}$ at 10 cm. (4-5 times worse for the B-layer) -> the noise occupancy must be below $10^{-6}$ hits/pixel/crossing.

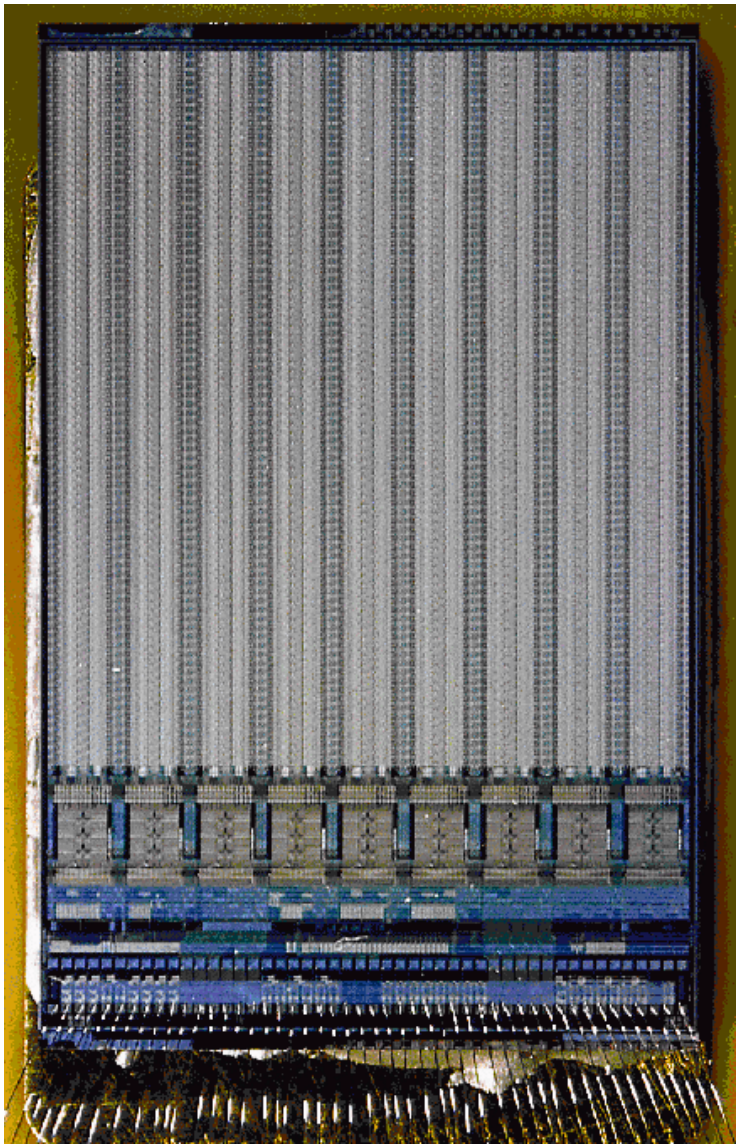
- Threshold of 3Ke with good enough timewalk to have ”in-time” threshold of about 4Ke (relative delay between large and small charge). This requires a small threshold dispersion (about 200e) and low noise (about 200e).

- Operate properly after total dose of 50 Mrad (nominal ATLAS 10 year dose). Also cope with expected sensor leakage currents of up to 50nA per pixel. For the B-layer, this corresponds to a live time of 2 years at design luminosity.

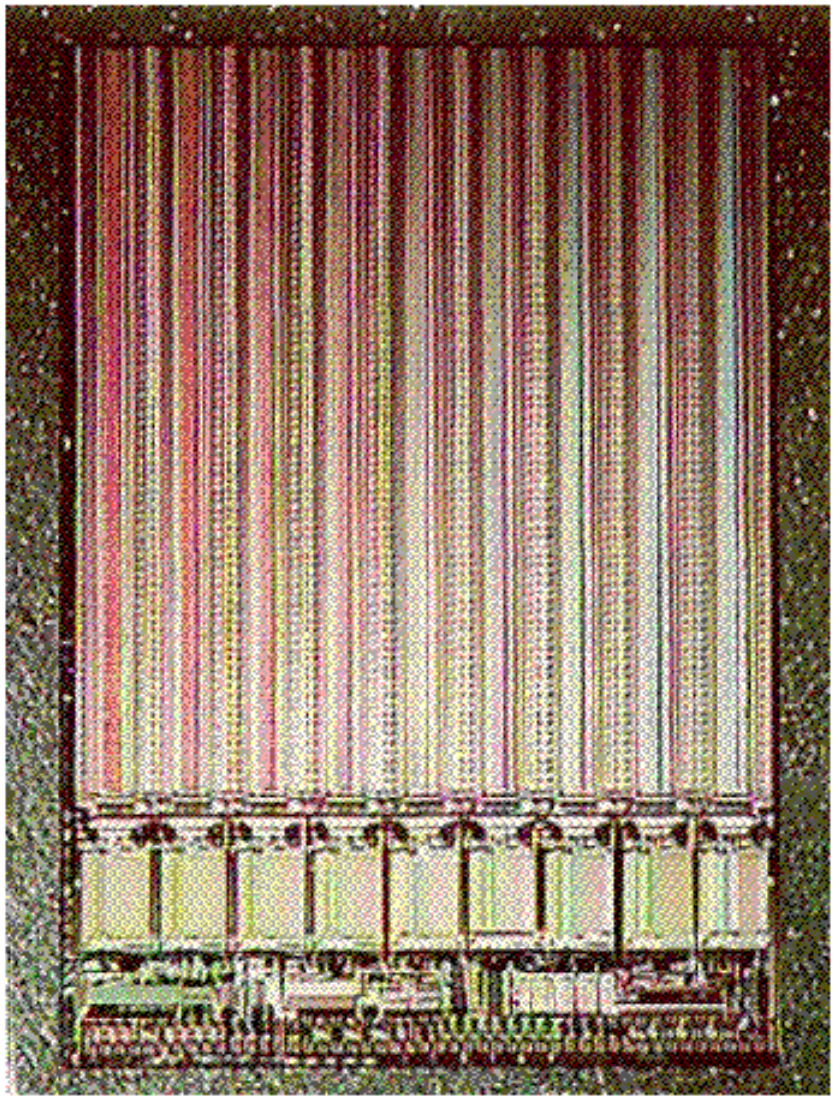
- Meet these specifications with an analog power budget of about 40μW/channel, i.e. 250mW for the FE-chip, i.e. 13kW for the entire pixel detector.

# General FE-chip features

- FE chip of 7.4 x 11.0mm die size with 7.2 x 8.0mm active area. (50μm x 400μm pixels arranged into 18 columns of 160 rows)
- Negative polarity fast preamps (for $n^+$ in $n^-$ sensor compatibility)
- Inputs and outputs signals are LVDS
- Serial command decoder (5MHz clock + data) implemented for minimal line-count
- Integrated DAC (8 x 8bit) providing the necessary front-end biases.
- Local data storage
- Serial data readout (at 40MHz) also for line reduction
- Each channel has its own dedicated 3-bit DAC for making minor threshold adjustments
- Integrated chopper circuit for providing fast test pulses of variable amplitude for the front-ends.
- 7-bit charge measurement using the Time-Over-Threshold technique.
- Fast-OR (Hitbus) from all channels providing a self triggering mechanism.
- Analog pream output providing monitoring for one channel.
- Individual pixel masking capability for both strobing and readout using a 2880-bit long shift register plus one latch per channel.



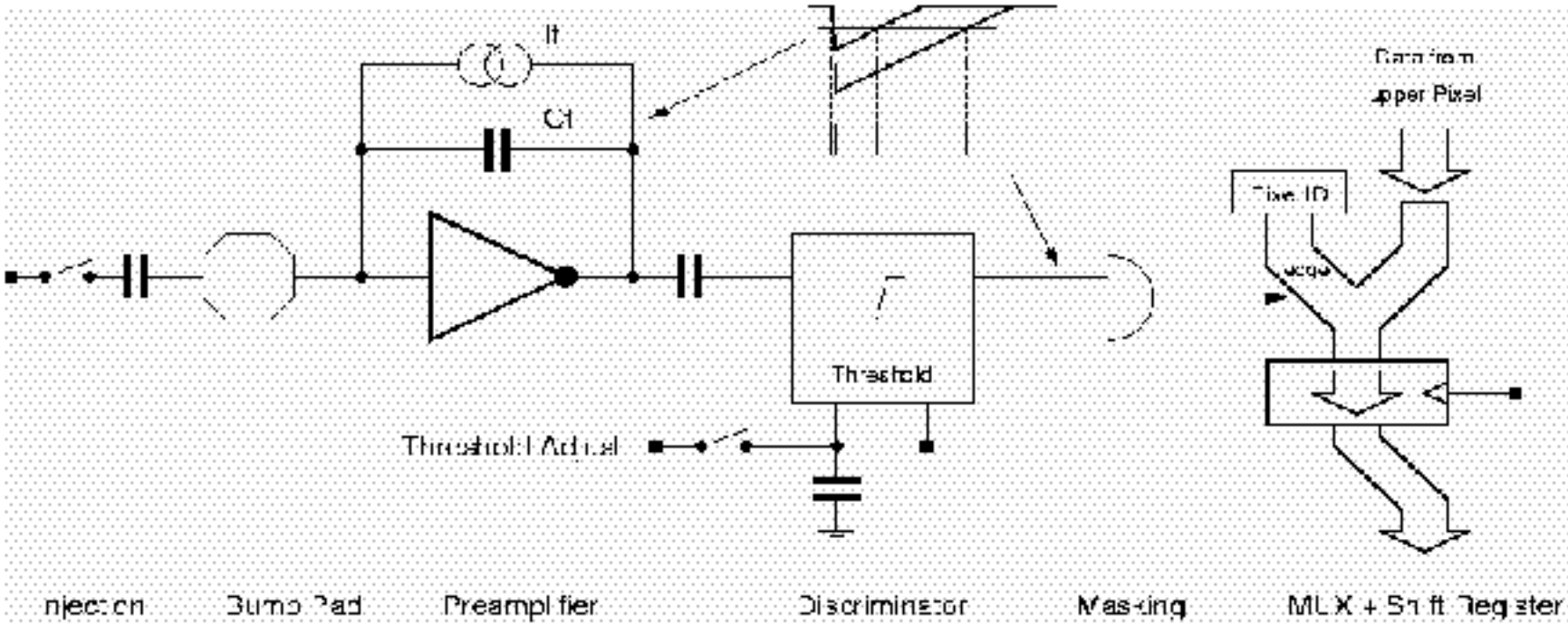
FE-A



FE-B

# FE-A & C

- Designed at CPPM and Universitat-Bonn, aimed for compatibility with DMILL
- FE-A incorporates bipolar front-end while FE-C is pure CMOS.
- Analogue front-end consists of a fast CSA incorporating a controllable DC feedback scheme
- Digital readout is based on 40 MHz dynamic shift register.

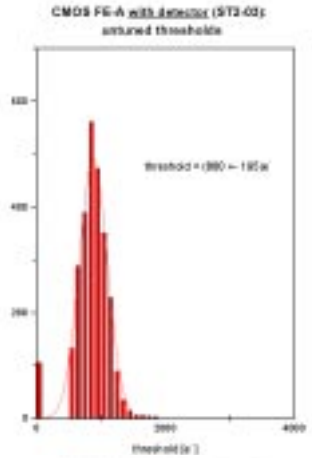


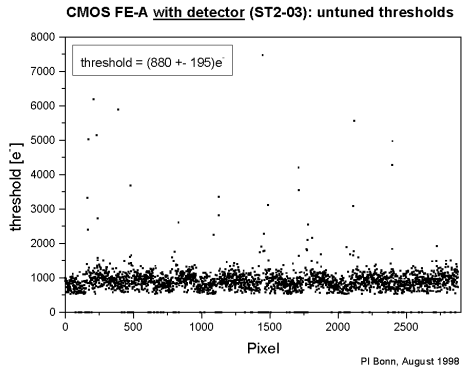
# FE-B

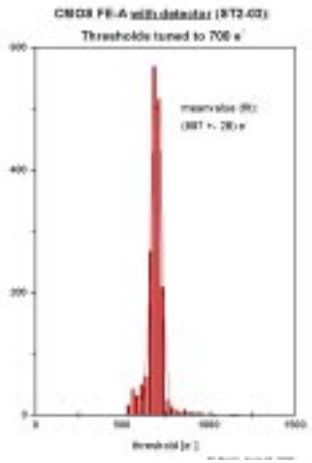
- Designed at LBNL, aimed for compatibility with Honeywell bulk and SOI process.
- Front-end is based on dual threshold discriminator.
- The readout architecture is also quite different from FE-A/C:
  - A 7 bit gray-code timestamp generator distributes global time. information throughout the array to each pixel.
  - Timestamp of leading-edge and trailing-edge are locally stored.
  - A continuous vertical sparse-scan seeks tagged hits along the column pairs.
  - Geographical and timing information is sent directly to the buffer pool at the bottom of the chip, where is stored for L1 latency, after which they are flagged for readout or deleted.
  - Chip transmits Trigger/Row/Column/TOT for each hit.

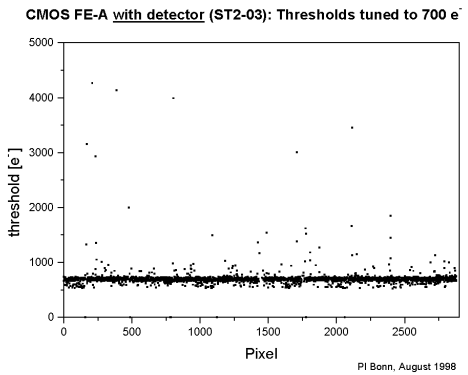
# Lab measurements

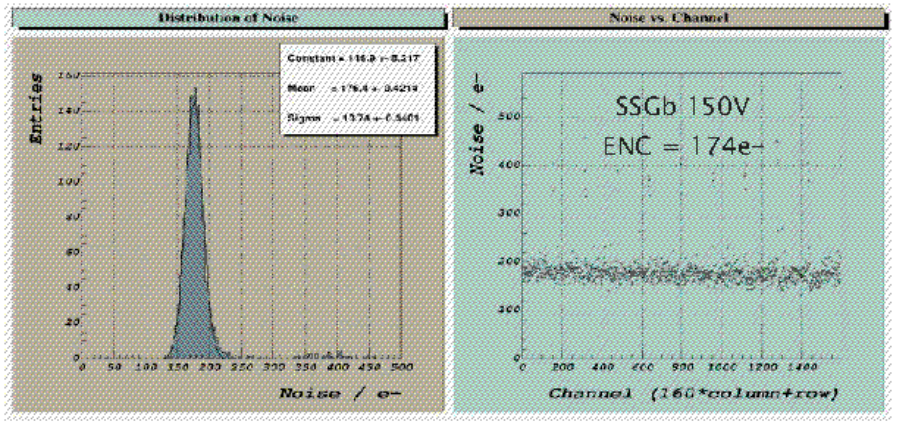
Examples of threshold and noise behavior in single chips:

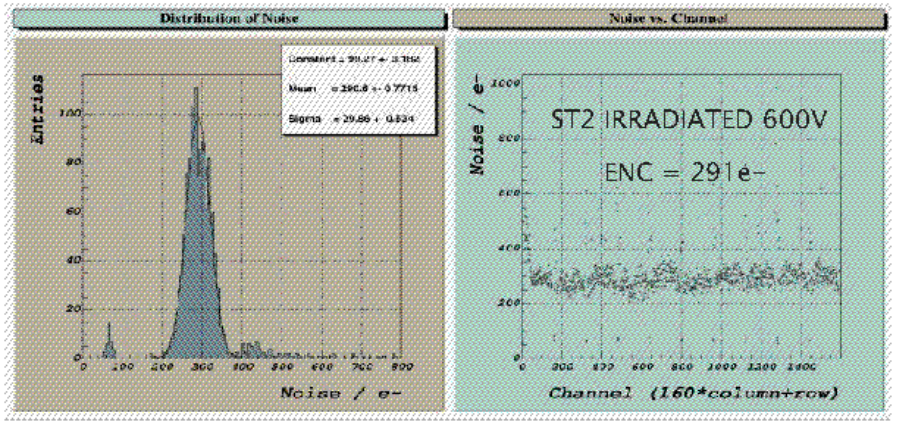







- Manage to achieve excellent dispersion when using individual trim DACs
- noise quite good even with irradiated sensors.

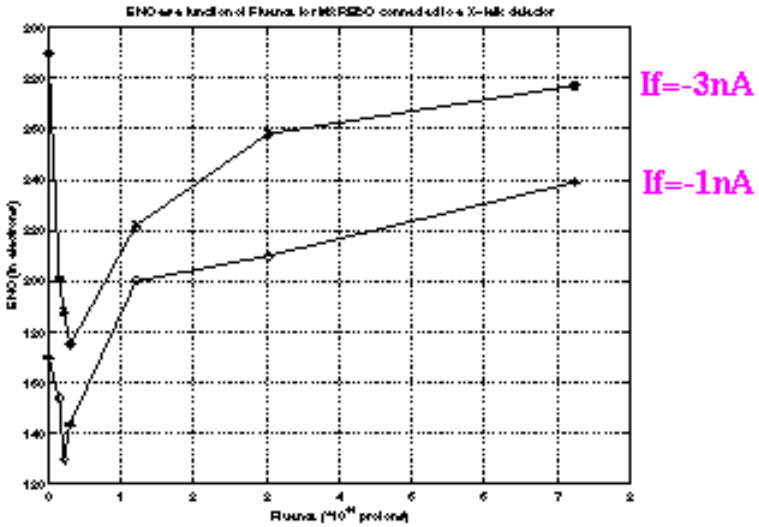
# Measurement on MAREBO+sensor during irradiation

The analog front-end is based on that of FE-A/C

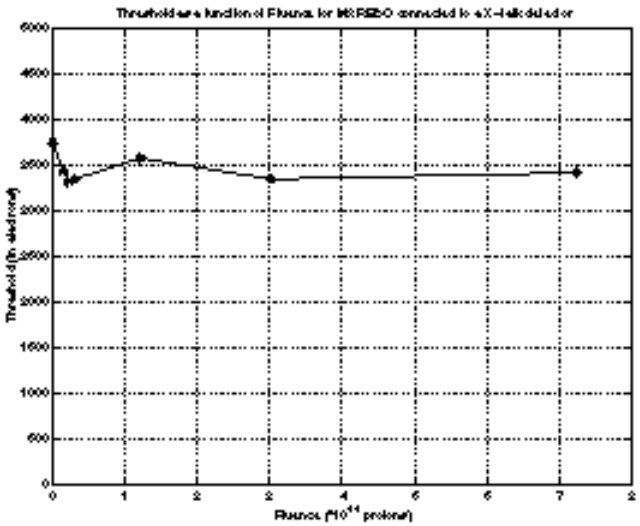
## SET-UP

- Irradiation at PS at CERN
- 24 GeV proton
- maximum flux 2.00 $10^{13}$ p $cm^{-2}h^{-1}$ (achieved with beam profile using a pixel)
- temperature of -7°C (monitored only inside the box)
- cooling box carried by a LABVIEW controlled movable stage
- In total, 6 irradiated MAREBO
  - 4 MAREBO with detectors (2 small-gap and 2 X-talk)
    - det2 measured on-line
  - 2 MAREBO without detector
    - one measured on-line

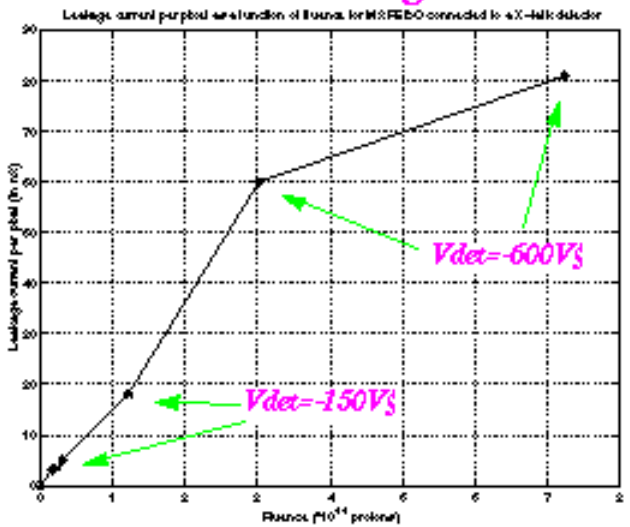
## Evolution of Noise



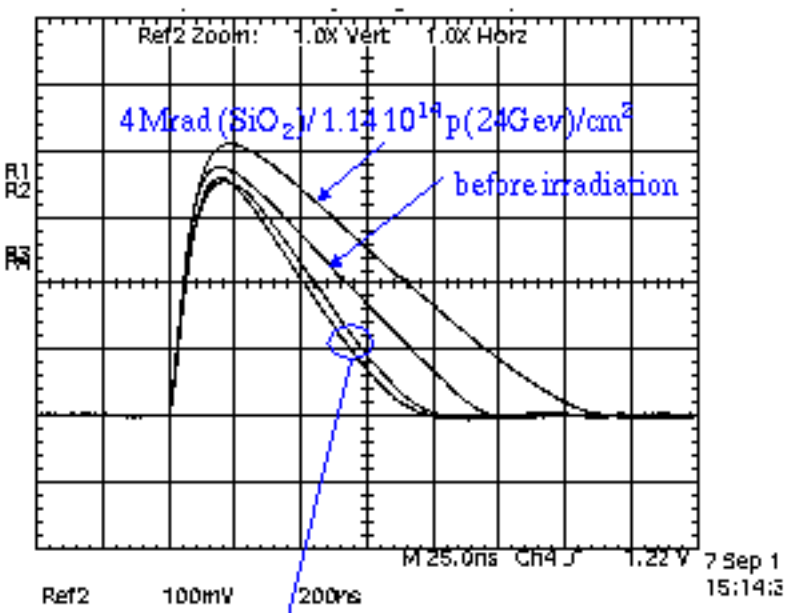

## Evolution of Threshold



## Evolution of Leakage Current



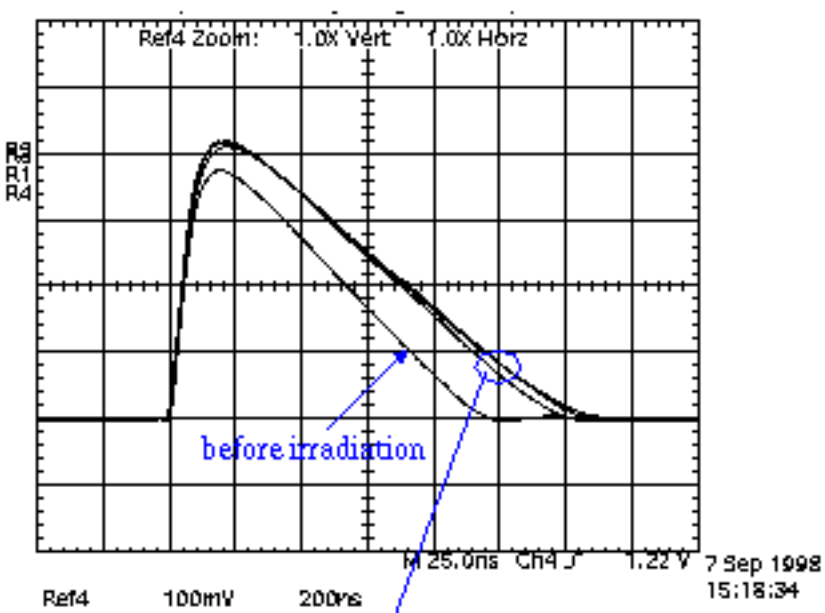
# Evolution of the output shape during irradiation




10 Mrad ($SiO_2$)/ 3 $10^{14}$ p(24Gev)/$cm^2$
ileak = 60 nA per pixel

24 Mrad ($SiO_2$)/ 7 $10^{14}$ p(24Gev)/$cm^2$
ileak = 81 nA per pixel

**Different steps during irradiation**




0.5 Mrad ($SiO_2$)/ 1.48 $10^{13}$ p(24Gev)/$cm^2$
ileak = 3nA per pixel

1 Mrad ($SiO_2$)/ 2.83 $10^{13}$ p(24Gev)/$cm^2$
ileak = 5nA per pixel

4 Mrad ($SiO_2$)/ 1.14 $10^{14}$ p(24Gev)/$cm^2$
ileak = 18nA per pixel

**Different steps during irradiation**

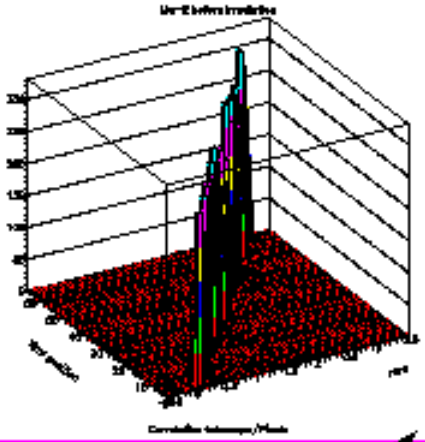
**INVERSION FLUENCE**: 8.7 $10^{13}$ p(24Gev)/$cm^2$

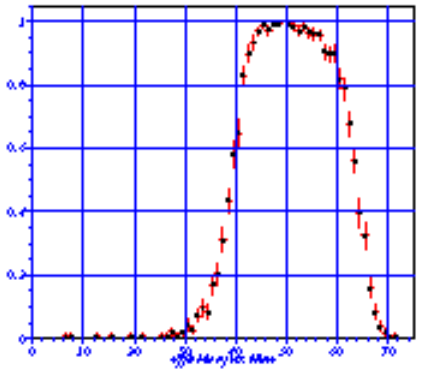
# MAREBO Testbeam studies

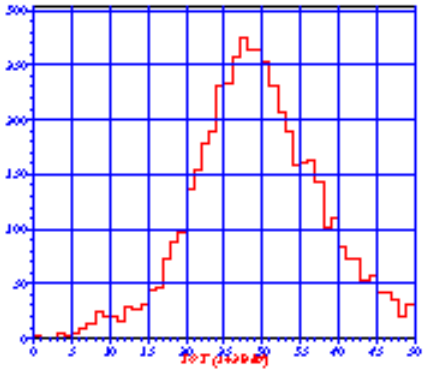
Correlation between pixel number and telescope prediction

Efficiency versus trigger delay

Analog information using the Time Over Threshold technique

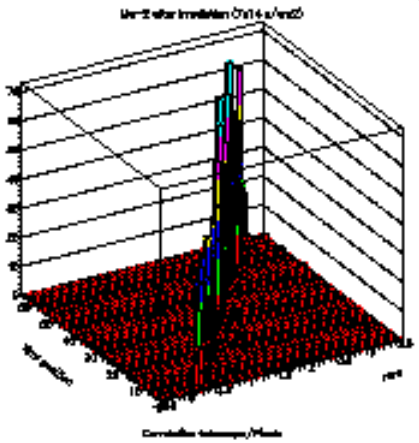


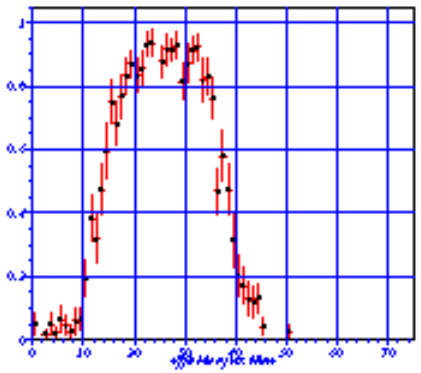


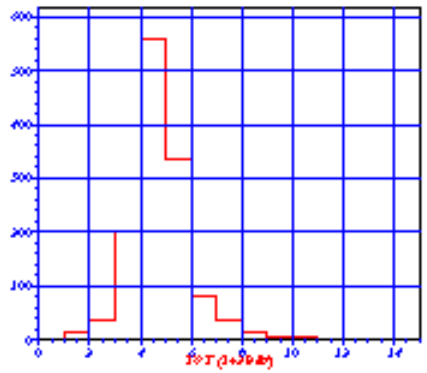


Threshold around 3500 $e^-$

BEFORE IRRADIATION







AFTER 24 Mrad ($SiO_2$)/ 7 $10^{14}$ p(24Gev)/$cm^2$ always at -7°C

# Radiation-Hard full arrays: FE-D & FE-H

Unified design approach adopted for rad-hard design FE chips => all working on same design to be implemented in two rad-hard processes

The rad-hard designs (FE-D in DMILL & FE-H in Honeywell SOI) maintains the spirit of the demonstrator programme (i.e. pin compatibility, same pixel pitches etc.) and combine features of both FE-A/C and FE-B.

DMILL: 0.8µm, 2 metal layers, incorporates CMOS, JFET and bipolar devices. 10Mrad tolerance guaranteed by the foundry but ATLAS prototyping has revealed radiation tolerance up to 30 Mrad.

Honeywell (SOI & bulk): 0.8µm, 3 metal layers, guaranteed up to 1 Mrad but independants evaluations have demonstrated a radiation tolerance at much higher doses

## FE-D (received in oct. 99)

- analog part

The front-end design is based on that of MAREBO/FE-A/FE-C with minor changes.

- absolute delay jitter has been fixed
- the layout has been squeezed in order to fit with the demanding 400µm length
  => has led to full CMOS design.
- the design and layout have been optimized for timewalk

- readout

derived from the FE-B architecture with some refinements:

- column readout bus now use low voltage swing for reduced digital pick-up, this necessitates the implementation of sense amps at the bottom-of-column logic.

- the end of column buffer pool has been increased to 24.

- other new features

- a self-trigger mode in which on recognition of a pulse on the global-OR (hitbus), the trigger sequence is automatically initiated once the requested latency period has elapsed.

- DACs are now formed from 2D array of current mirrors for monotonic behavior and for radiation tolerance.

## FE-H ( to be submitted in summer)

The same design adapted for the Honeywell SOI process is in preparation.

# Concluding

- The radiation-soft phase of the demonstrator programme has enabled us to successfully evaluate 2 design approaches in great detail using two reliable technologies. This in turn led us to a single layout for the first full-scale radiation hard submission.
- All of the critical (non rad-hard) ATLAS FE specs such as efficiency, power consumption, resolution, threshold dispersion, noise, crosstalk have been demonstrated.
- Tests on FE-D show up a peculiar low yield in 2 locations of the chip. Extensive lab measurements have enabled to isolate faulty transistors and to get more insight into the failure mechanism. A close study between TEMIC and labs is being pursued.